BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

FIG. 1 is a cross-sectional view of a prior art liner/barrier/seed process that results in an overhang of material at the top of a trench, via, or contact;

FIGs. 2A-2E are cross-sectional drawings of a copper interconnect structure formed according to the first embodiment of the invention; and

FIGs. 3A-3D are cross-sectional drawings of a contact structure formed according to a second embodiment of the invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

Several embodiments of the invention are discussed below. The invention uses a light sputter etch with low bias to remove or reduce the overhang typically associated with a PVD liner/barrier/seed layer. The sputter etch is performed after the deposition of the liner/barrier/seed layer. No sputtering of the dielectric is performed. Therefore, redeposition of dielectric material is avoided.

The first embodiment of the invention will now be discussed in conjunction with a dual damascene copper interconnect process. It will be apparent to those of ordinary skill in the art that the benefits of the invention may be applied to other interconnect processes in which a PVD liner/barrier is deposited over a narrow opening. The first embodiment is discussed with reference to FIGs. 2A-2E.

A semiconductor body 100 is processed through formation of trench and vias in a metal interconnect level, as shown in FIG. 2A. Semiconductor body 100 typically comprises a silicon substrate with transistors and other devices formed therein. Semiconductor body 100 also includes the pre-metal dielectric (PMD) and may include one or more metal interconnect layers.

An ILD (interlevel dielectric) 102 is formed over semiconductor body 100. IMD (intrametal dielectric) 104 is formed over ILD 102. An etchstop layer (not shown) may optionally be placed between ILD 102 and IMD 104. Suitable dielectrics for ILD 102 and IMD 104, such as silicon dioxides, fluorine-doped silicate glass (FSG), organo-silicate glass (OSG), hydrogen silesquioxane (HSQ), and combinations thereof, are known in the art. ILD 102 and IMD 104 are thick dielectric layers having a thickness in the range of 0.1 um – 1 um.

In a copper dual damascene process, both the vias and trenches are

etched in the dielectric. Via 106 is etched in ILD 102 and trench 108 is etched in IMD 104. Via 106 is used to connect to underlying metal interconnect layers. Trench 108 is used to form the metal interconnect lines.

Liner/barrier layer 110 is deposited using a PVD process over IMD 104 including in trench 108 and via 106, as shown in FIG. 2B. Liner/barrier layer 110 functions to prevent copper diffusion into the ILD and IMD layers. For example, liner/barrier layer 110 may comprise Ti or TiN. Other suitable liner/barrier materials such as Ta, TaN, TiN, TaNSi, TiNSi, MoN and WN are known in the art. Due to the nature of the PVD process, the thickness of the liner/barrier layer 110 is greater at the top of trench 108 and via 106. This is referred to as an overhang 111.

In a copper interconnect process, a copper seed layer 112 is deposited over liner/barrier layer 110. Seed layer 112 is typically deposited using a PVD process. Accordingly, overhang 111 includes excess seed material as well.

In the preferred embodiment, after the seed layer 112 is deposited, a sputter etch is performed to remove/reduce overhang 111, as shown in FIG. 2C. Alternatively, the sputter etch may be performed between the liner/barrier deposition and seed deposition steps. The sputter etch uses a low bias (e.g., 0 volt to -300 volts) to improve the film profile. By using a low bias, only the metal in the field and top corners is removed. The bottom film thickness does not change significantly and therefore, the amount of material at the bottom interface is preserved. The sputter etch is preferably performed in situ after the liner/barrier/seed deposition without breaking vacuum to preserve the film's integrity.

The duration of the sputter etch is chosen such that the corners of the trench 108 or via 106 are not exposed. Sufficient liner/barrier material 110/112